Design automation of ΔΣ switched capacitor modulators using SPICE and MATLAB

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***Abstract*—Concerning the fact that the design of contemporary integrated circuits (IC) is practically impossible without using sophisticated Electronic Design Automation (EDA) software paper gives some interesting thoughts and considerations about this issue. As technology processes advances on year basis consequently EDA industry is forced to follow this trend as well. This, on the other hand, requires IC designer to frequently and efficiently accommodate to new working environments. Authors of this paper hopes that ideas and some of early results which are to be presented helps in dealing with this sensitive matter of EDA especially when large and functionally demanding mixed-signal blocks are under consideration. As an example second order ΔΣ modulator is treated with proposed EDA procedure to illustrate possible simulation time saving which is more than welcome in a world of analog and mixed-signal design.**

***Index Terms*—Electronic Design Automation; modeling; ΔΣ modulation; analog and mixed-signal circuitry**

I. Introduction

IT is not needed to specially explain that now days EDA in IC design is not luxury by contrast it is necessity. Leading EDA software development companies such as Cadence® and MentorGraphics® invests numerous amounts of financial and intellectual means to provide quality and efficient software environments. These environments implement complex algorithms such as equation solvers, floor planers, routers etc. All this puts additional work load and mental labor to an IC designer. Therefore in order to successfully design and prepare (implement) chip besides theoretical and practical knowledge about circuit operation additional effort has to be invested. This implies multidisciplinary diapason ranging from numeric, programming/scripting skills and efficient algorithm development all the way to background understanding of target technology process. This requires additional knowledge from world of computer science that electronic circuits designer/engineer has to adopt. Unfortunately, even though modern EDA tools provide excellent design automation possibilities they are usually very expensive and unavailable for smaller design teams/companies. As previously mentioned problem arises when functionally complex analog and mixed-signal blocks are considered. Therefore high-level modeling approach of such complex blocks has to be introduced. Now days there are numerous high-level modeling Hardware Description Languages (HDL) such as Veriolog-AMS, Verilog-A, VHDL-AMS, System Verilog, SystemC etc. All of these HDLs provide many high-end capabilities and practically defines a standard in high-level modeling. However software support (Integrated Design Environment-IDE, compilers, solver engines etc.) are again covered with very expensive licensing policy.

This issue provokes science community to get around it and come up with appropriate EDA environment which will save design time but still preserve dissent amount of accuracy. There are two aspects that EDA should support. First, Top-Down methodology, where it supposes to help circuit designers to extract key design parameters bringing them closer to the physical realization. And second, Bottom-Up methodology, when finished designs have to be characterized to provide as accurate as possible model which will serve in system-level design. Concerning this second aspect, remarkable results for Continuous Time (CT) class of circuitry is accomplished in [1]. Nice thing about CT circuits is that the designer does not have any hard constraint when choosing type of the simulation to use. In other words one can usually use all from the simulator set i.e. operation point (quiescent), transient, DC and AC. Of course the best insight into circuit operation gives transient analysis but it consumes large amount of the design time.

Now, what about Discrete-Time (DT) analog and mixed-signal blocks? The most popular realization of this type of circuitry in CMOS processes is with Switched Capacitor (SC) circuitry. But now one no longer has the comfort of using all types of simulation from the set. Moreover only transient analysis is available since switching operation is present therefore e.g. AC analysis is not applicable. Unfortunately these are the longest one and the time to characterize circuit's behavior or to extract key design parameters for it becomes a prime parameter to minimize. Therefore this paper proposes the way to automate the design process of SC topologies using less expensive or even free programming and CAD tools. Here free SPICE platform in conjunction with appropriate MATLAB scripts is used. It is not necessary to explain that every analog and mixed-signal designer possess knowledge about analog circuit simulation hence SPICE is adopted as simulation platform. Taking into account the type of the circuit, free version of SPICE optimized for switched regulators provided by Linear Technology Inc is adopted [2]. For design automation, MATLAB platform is chosen because

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it is widespread in engineering community and it certainly drops in to the spectrum of engineering skills. Practically even free version of MATLAB (or its free derivatives such as FreeMat, Octave) can provide quite respective signal processing, data management and data presentation capabilities. All this makes these two software tools attractive ingredients for building an inexpensive, custom EDA platform.

First section covers basic background of second order ΔΣ CIFF (Cascade of Integrators Feed-Forward) architecture with emphasis on realization i.e. SC topology. Soon after, in second section, modeling approach of such circuitry with non-idealities is to be discussed. The adopted target parameters for figure of merit are covered as well. Third section explains proposed EDA procedure and strategy for its realization. Fourth section presents some of the preliminary simulation results which illustrate functionality of the prototyped EDA platform. Finally, findings and further development directions of proposed EDA platform are sublimated in the conclusion.

II. Model of Second Order ΔΣ CIFF Modulator

As the circuit example second order ΔΣ CIFF modulator is chosen. This architecture is quite attractive in design of ΔΣ ADCs. More about system level analyses and simulation of this architecture can be found in [3]. Here, focus is on realization. Since detailed schematic of fully differential topology is reported in [4] only conceptual illustration of the schematic is presented in fig. 1.

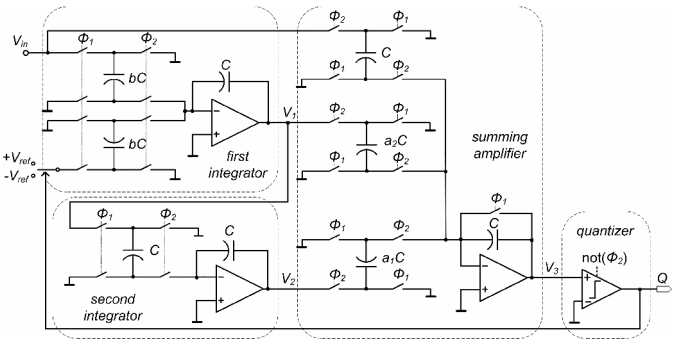

Fig. 1. Simplified schematic of second order ΔΣ CIFF modulator

Fig. 1 represents single sided topology with common mode voltage at ground potential. This realization provides second order, Z-domain, High Pass (HP) noise transfer function (NTF) given in (1).

$$NTF(z) = \frac{z^2 - 2z + 1}{(z - p_1)(z - p_2)} \tag{1}$$

Here p_1 and p_2 are poles of the function with values $0.3819 \pm j0.3004$ [5]. This circuit should provide about 80dB signal-to-noise ratio (*SNR*) by pushing (shaping) the in-band noise in higher frequencies while preserving spectral content of useful, low frequency signal. Table I summarizes adopted basic design parameters of the modulator.

TABLE I
Modulator's Basic Parameters

Parameter	Description	Value
a_1	coefficient	11/3
a_2	coefficient	4/3
b	coefficient	1/3
OSR	oversampling ratio	256
BW	base bandwidth	24 kHz
C	feedback capacitance	1.7 pF
V_{ref}	reference voltage	0.6 V
V_{FS}	full-scale voltage	0.8 V
f_s	sampling frequency ($\Phi_{1/2}$ clock)	12.6 MHz

As usual SC circuits operate in two non-overlapped clock phases, Φ_1 and Φ_2 at frequency f_s. In phase Φ_1 charge proportional to input voltages in SC integrators is stored at input capacitors while capacitors in the summing amplifier are discharged. During the second, Φ_2 phase output voltages of integrators, V_1 and V_2, are evaluated by passing the accumulated charge to integrator's feedback capacitors. These voltages are then summed with input voltage, V_{in} in SC summing amplifier producing V_3. Since in phase Φ_2 a new value for outputs in SC circuits is determined, quantizer output Q has to be stable at that time in order to provide whether plus or minus V_{ref} at the input of the first integrator. Therefore clock signal not(Φ_2) sets the quantizer output.

Even functionality of the circuit can be easily lexically described it is not a trivial task in time domain. As one can see from fig. 1 there are a lot of switches which operate at high frequency. Effects like KT/C noise and clock feed through arise in this case. Hence, robust time domain model of the modulator is developed. Modulator is modeled in SPICE using adequate dependent sources and passive primitives, like resistors and capacitors, and active primitives like switches with finite on/off resistance. Operational Transconductance Amplifier (OTA) model includes: finite DC gain; finite bandwidth; slew rate; tail current of differential par and noise sources. These are the key design parameters for OTA which has to be known before circuit designer can start transistor level design. Therefore extensive time domain, parametric, simulations hast to be performed to extract them. Initial OTA parameters are given in the Table II.

It is obvious that the model by its self is already complicated structure. There are a lot of nodes for which voltage/current values has to be calculated with maximally $1/f_s$ time step. Considering the circuit's operation, changes of these values are usually stepwise with change of sign. This consequently may easily lead to divergence problems. Hence

special care has to be devoted to setting simulator options and initial conditions primarily for capacitors. Finally output of the quantizer produces discrete values form the set $\{0, V_{DD}\}$, i.e. {0, 1} in digital domain, at every $1/f_s$ seconds. Therefore only way to evaluate circuit's behavior is FFT analysis which requires at least $64 \cdot OSR$ (16384 for OSR =256) points to do the job [6].

TABLE II
OTA'S INITIAL PARAMETERS

Parameter	Description	Value
A_{dc}	DC gain	80dB
slr	slewrate	1.26 V/ns
f_{gbw}	Gain bandwidth product	1.26 GHz
v_n	Max offset noise amplitude	6.1 µV
v_{nktc}	Max KT/C noise amplitude	6.1 µV
I_0	Max diff. par tail current	100 µA
V_{DD}	power supply voltage	1.2 V
V_{CM}	common mode voltage	0.6 V

All this results in long simulation time and developed behavioral model should help minimize it while providing extraction of OTA's design parameters. Following section will describe automation procedure in more detail.

III. EDA PROCEDURE FOR SECOND ORDER ΔΣ CIFF MODULATOR

Extraction process requires a lot of file management work which is usually done manually hence the idea to automate the process in order to ease the engineer's workload. Basically in order to extract OTA's parameters one has to begin with initial, nearly ideal, model parameters, run a time domain simulation, process output data i.e. calculate FFT, evaluate *SNR* and plot spectrum as a figure of merit for the circuit. Then the decision has to be made which model parameter to loosen in order to make it realizable and repeat the process i.e. run simulation and again calculates *SNR*. Finally ideal and non-ideal *SNR*s and spectrums are compared to check whether the requirements are met and this should be done for all model parameters. It is not hard to prove that for at least five OTA model parameters with e.g. five possible values for each of them we need ten time domain simulations. This would require designer to run parametric simulation and store result in separate files/locations for each parameter and then to process individual files thorough available scripts and finally represent the data in order to get insight in circuit behavior. It is clear that this represent tedious work prone to errors. Therefore fig. 2 illustrates possible solution for automation.

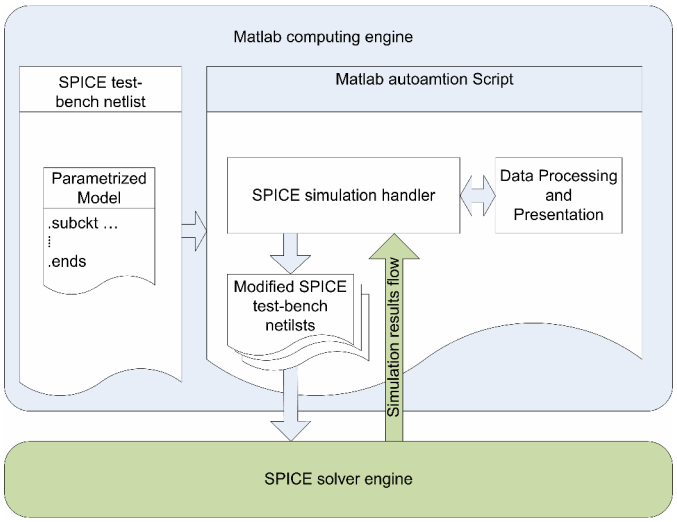

Fig. 2. Illustrative block diagram of proposed EDA procedure

The whole process of automation has been entrusted to MATLAB computing engine (MCE). Appropriate script is written which can be roughly divided in two main sub-blocks of code. First is in charge for running and monitoring SPICE engine and data management of obtained simulation results hence the name SPICE simulation handler (SSH). Second, called Data Processing and Presentation (DPP), serves as post-simulation data processor and presenter. Here all substantially important data processing e.g. parsing, FFT computation and SNR estimation takes place. Main input argument that is required is SPICE test-bench netlist in which ΔΣ model is built-in. After accepting this netlist SSH will produce multiple versions of it with given model parameter values and call SPICE solver engine (SSE). One by one modified test-bench netlists are passed to SSE and transient analysis is performed. SSH then needs to monitor SSE in order to detect simulation end, collect obtained data and, if necessary, run the simulation again. This is the most delicate block of the script code because it mast successfully handle with tools connection point.

One can easily notice that there is no decision block in fig. 2. It should be emphasized that this is an early version of software which for now serves to confirm the automation process idea. Therefore optimization algorithm for OTA's design parameters is not implemented, and software still requires some interaction with the user. This primarily applies to manually assigning a new set of model parameter values. At this stage of software development one set of values for one parameter is allowed in one run. After completion of first parametric simulations set script has to be restarted to assign a new set of values for some other parameter. Strategy for choosing which parameter next to vary is left for the user to decide. Anyway, engineer is released of tedious data

management work which was the goal in the first place.

Some of the preliminary obtained results are presented in the following section in order to support and clarify the previous talk.

IV. Simulation Results

This section presents some of the early results. First numeric model, also coded in MATLAB script, is used to simulate ideal behavior of second order CIFF architecture. It cannot be emphasized enough how important is to properly choose frequency of input test sinusoid signal and appropriate windowing function. This choice is so critical that can make or break spectral estimation of the output signal. Since that is out of the scope of this paper reader is advised to look [6]. Adopted parameters for performing FFT analysis are given in Table III.

TABLE III
FTT Analysis Parameters

Parameter	Description	Value
N	FFT length	16384
f_{in}	test signal frequency	3.84 kHz
V_{in}	test signal amplitude	0.4 V
window	windowing function	Hann

Ideal behavior of the second order CIFF is shown in fig. 3.

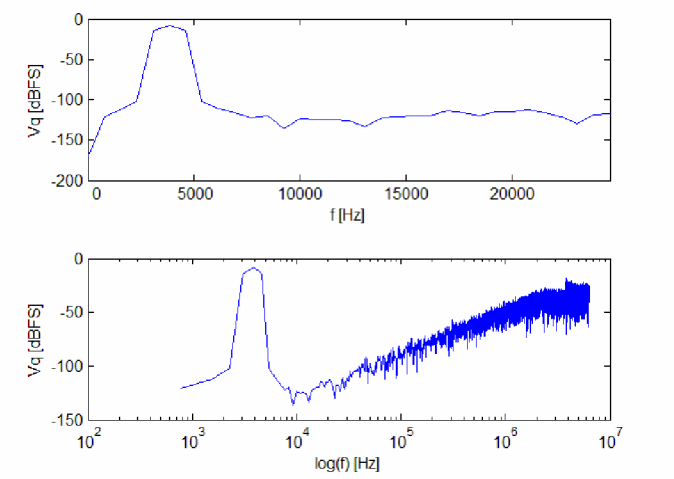

Fig. 3. FFT spectrum of the second order CIFF output

Upper plot in Fig. 3 shows spectrum with linear scale for frequency axis limited to base band i.e. 24 kHz. Lower plot represents the same spectrum in log-log scale where +40dB/dec out of band HP slope is evident. In both cases ordinate axis are represented in dBFS i.e. decibels in full-scale to emphasize that input is fed with V_{FS}. Obtained value at f_{in} bin is -7.959dBFS which corresponds to 0.4 V amplitude of input signal. In this, ideal, case *SNR* is estimated to 91.34dBs.

Fig. 4 show results obtained using developed EDA script and behavioral SPICE model of the ΔΣ structure with non-idealities. In this test case f_{gbw} is set to 126 MHz, and $slr = k_{slr}$·(12.6 V/µs), where $k_{slr} \in \{100, 10, 1, 0.1\}$. All other OTA parameters are left as in Table II.

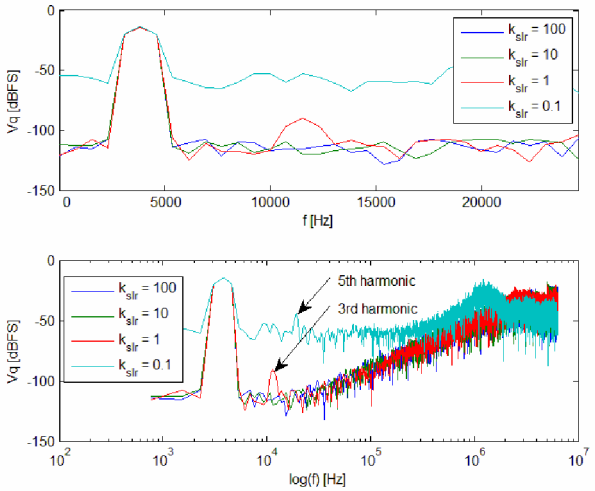

Fig. 4. FFT spectrum of the second order CIFF output

Observing fig. 4 one can see that for 1.26 V/ns and 0.126 V/ns *slr* values modulator still operates normally. When *slr* drops to 12.6 V/µs healthy operation is preserved but there is a rise of third harmonic. In this case *SFDR* (Spurious Free Dynamic Range) which represents ratio of main and third harmonic is estimated to 76.47dBs. For lowest slewrate value, *slr* = 1.26 V/µs, function of the circuit is significantly distort plus fifth harmonic showed up. Estimated *SNR* values corresponding to decreasing *slr* are 84.75, 84.57, 84.29 and 31.27 dBs. Since required *SNR* is 80dB one can conclude that, if all fixed OTA parameters are realizable and obtained *SFDR* is tolerable, *slr* of 12.6 V/µs is acceptable even with third harmonic present. It is also important to notice that value of main harmonic at f_{in} is -13.77dBFS which is about 6dBs lower than in the ideal case. This indicates that probably modulator coefficients should be rescaled.

All these analysis are performed in significantly short time. Total simulation time in this case for four *slr* values i.e. four transient simulations is about half an hour. Concerning that one transistor level transient simulation of such circuit can easily last for whole day or two depending on computing power of exploited hardware platform. Therefore time savings are tremendous.

V. Conclusion

The paper's prime goal is to stress importance of EDA in electronic circuit design and offer usable solution. Challenges and aspects of EDA software development are commented first. Problems concerning simulation of complex mixed-signal blocks are emphasized as well. Representative example of second order CIFF ΔΣ modulator is presented. Modeling approach of such circuitry is discussed as well. Proposed EDA procedure is explained. Early version of developed software which implements proposed EDA procedure is described. Simulation results confirmed model validity and justified proposed EDA procedure. Significant simulation time saving is obtained.

It is also proved that decent EDA tool can be developed using low cost or free software platforms. In future work this prototype version of software should be improved in both flexibility and appearance. Firs effort should be put in exploring possibilities for implementing some kind of optimization algorithm for OTA parameters. For now software is available in script i.e. low level form. When software becomes functionally mature development of more sophisticated user interface will be considered.

Acknowledgment

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